BENHA UNIVERSITY
FACULTY OF ENGINEERING (SHOUBRA)
ELECTRONICS AND COMMUNICATIONS ENGINEERING

ECE 444
Industrial Electronics

(2022 - 2023) 1st term

Lecture 5: Digital Signal Conditioning.

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Outlines:

- Introduction.
- Converters.
- Comparator.
- Digital-to-Analog Converters (DACs).
- Analog-to-Digital Converters (ADCs).

Introduction

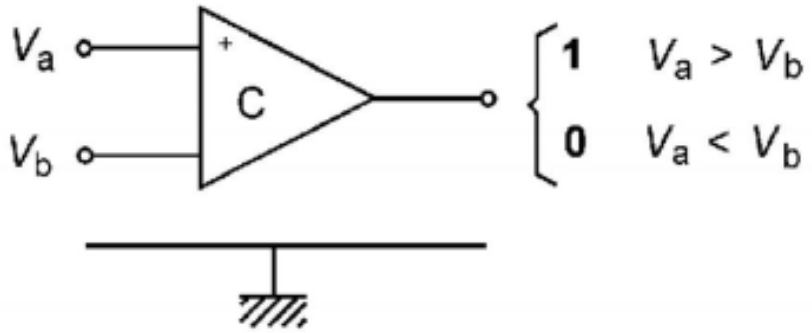
- Why using digital signal?
  - Reduction of uncertainty.
  - Reduction of size, power consumption & failure rate.
  - Using computers (in many form) in control enable implementation of:
    - ✓ Multivariable control
    - ✓ Software linearization of sensor output
    - ✓ Solving complicated control equations and modification as needed
    - ✓ Using networking for large process complex.

Converters

- Most measurements of process variables are performed by devices that translate information about the variable to an analog electrical signal.
- To interface this signal with a computer or digital logic circuit, it is necessary first to perform an analog-to-digital (A/D) conversion.
- Often, the reverse situation occurs, where a digital signal is required to drive an analog device. In this case, a digital-to-analog (D/A) converter is required.
- The specifics of this conversion must be well known.

Comparator

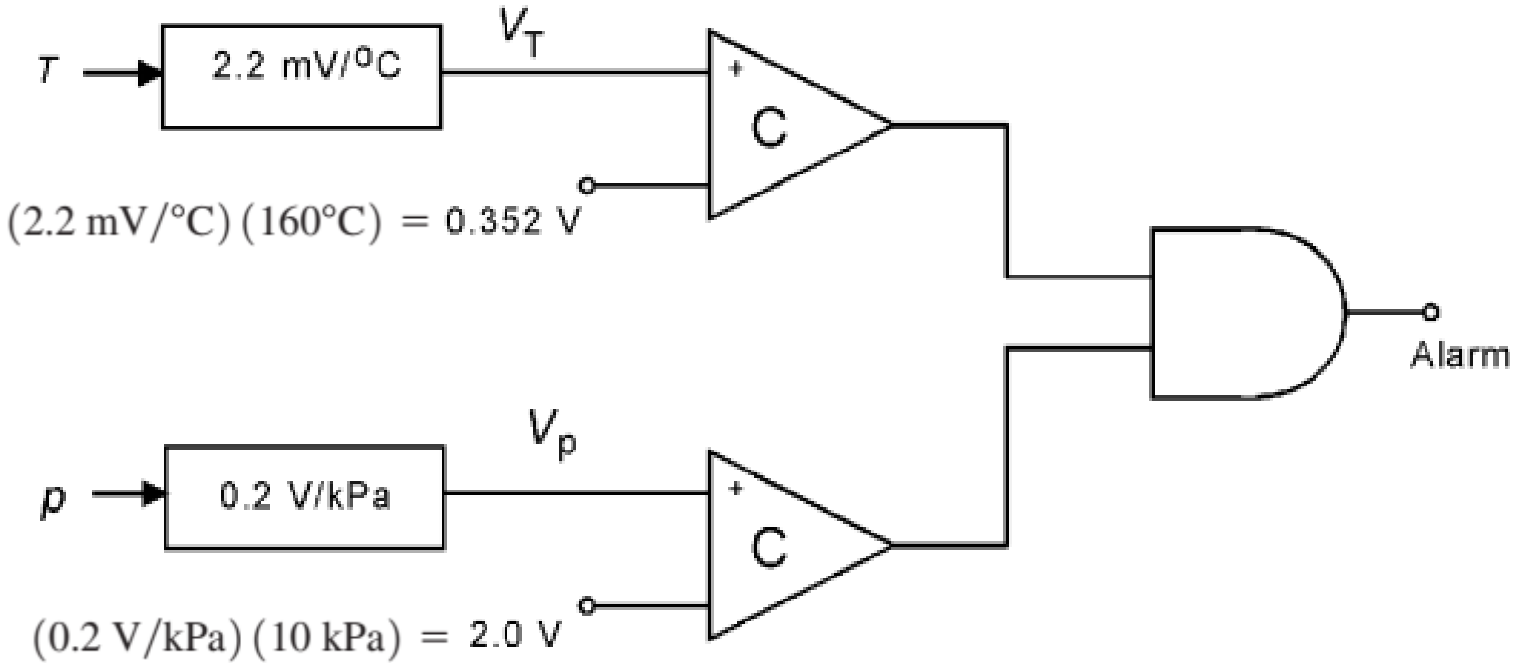
- A basic comparator compares voltages and produces a digital output.
- Simply compares two analog voltages on its input terminals. Depending on which voltage is larger, the output will be a 1 (high) or a 0 (low) digital signal.
- The comparator is extensively used for alarm signals to computers or digital processing systems.



Converters

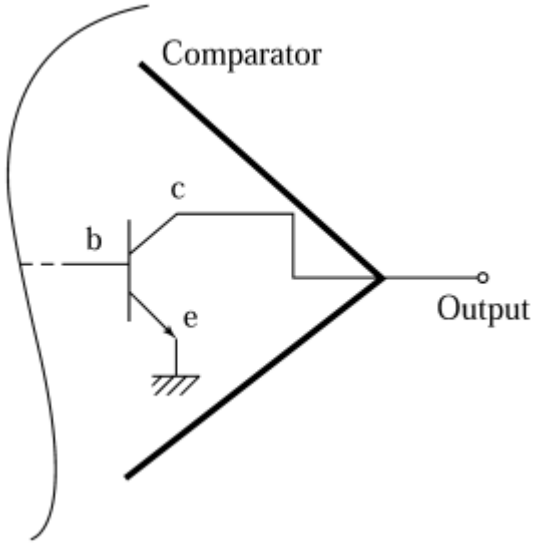
EXAMPLE 7 A process-control system specifies that temperature should never exceed 160°C if the pressure also exceeds 10 kPa. Design an alarm system to detect this condition, using temperature and pressure transducers with transfer functions of 2.2 mV/°C and 0.2 V/kPa, respectively.

Solution

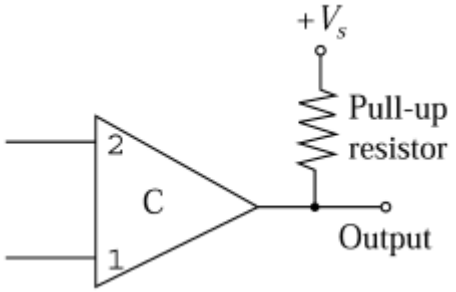


Open Collector Output

- Of course, even if there is base-emitter current in the transistor, no voltage will show up on the collector until it is connected to a supply through some collector resistor. In fact, this is exactly what is done when an external resistor is connected from the output to an appropriate power supply. This is called a collector pullup resistor.

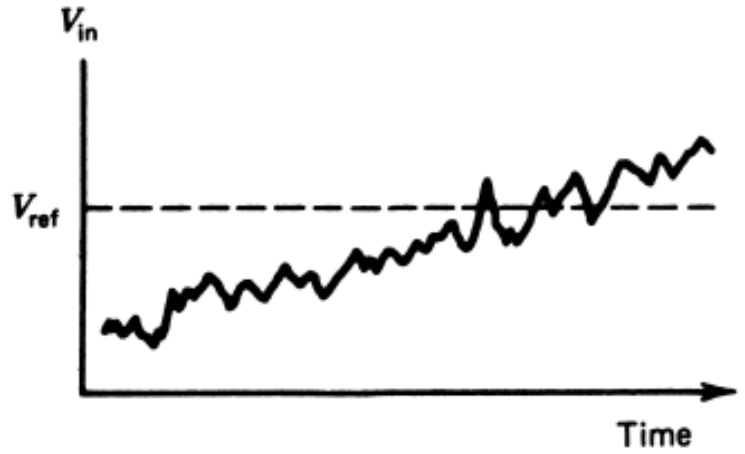


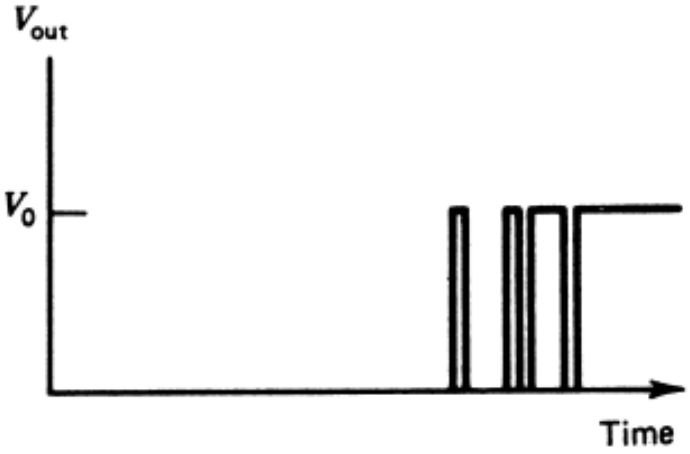
- Advantages to using the open-collector output:
  I. It is possible to use a different power source for the output.
  II. It is possible to OR together several comparators' outputs.

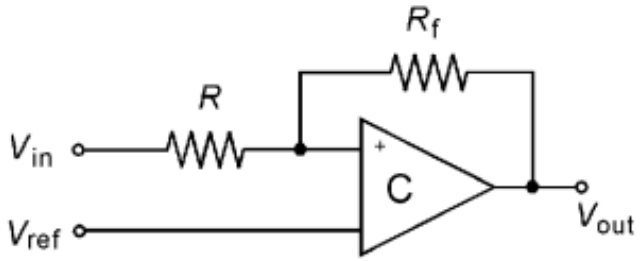


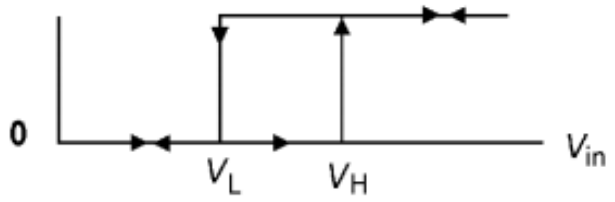
Hysteresis Comparator

- When using comparators, there is often a problem that the comparator output may "jiggle" back and forth between high and low as the reference level is reached.
- This problem can often be solved by providing a hysteresis window to the reference level around which output changes occur.
- Once the comparator has been triggered high, the reference level is automatically reduced.









$$V_L = V_{ref} - \frac{R}{R_f} V_0 \qquad V_H = V_{ref}$$

Converters

EXAMPLE 8 A sensor converts the liquid level in a tank to voltage according to the transfer function (20 mV/cm). A comparator is supposed to go high (5 V) whenever the level becomes 50 cm. Splashing causes the level to fluctuate by ±3 cm. Develop a hysteresis comparator to protect against the effects of splashing.

Solution

The nominal reference for the comparator occurs at 50 cm,

$$V_{\text{ref}} = (20\ \text{mV/cm})\,(50\ \text{cm}) = 1\ \text{V}$$

The splashing, however, causes a "noise" of

$$(20\ \text{mV/cm}) \cdot (\pm 3\ \text{cm}) = \pm 60\ \text{mV}.$$

This is a total range of **120 mV**. We need a deadband of at least 120 mV, but let us make it **150 mV** for security. Thus, we have

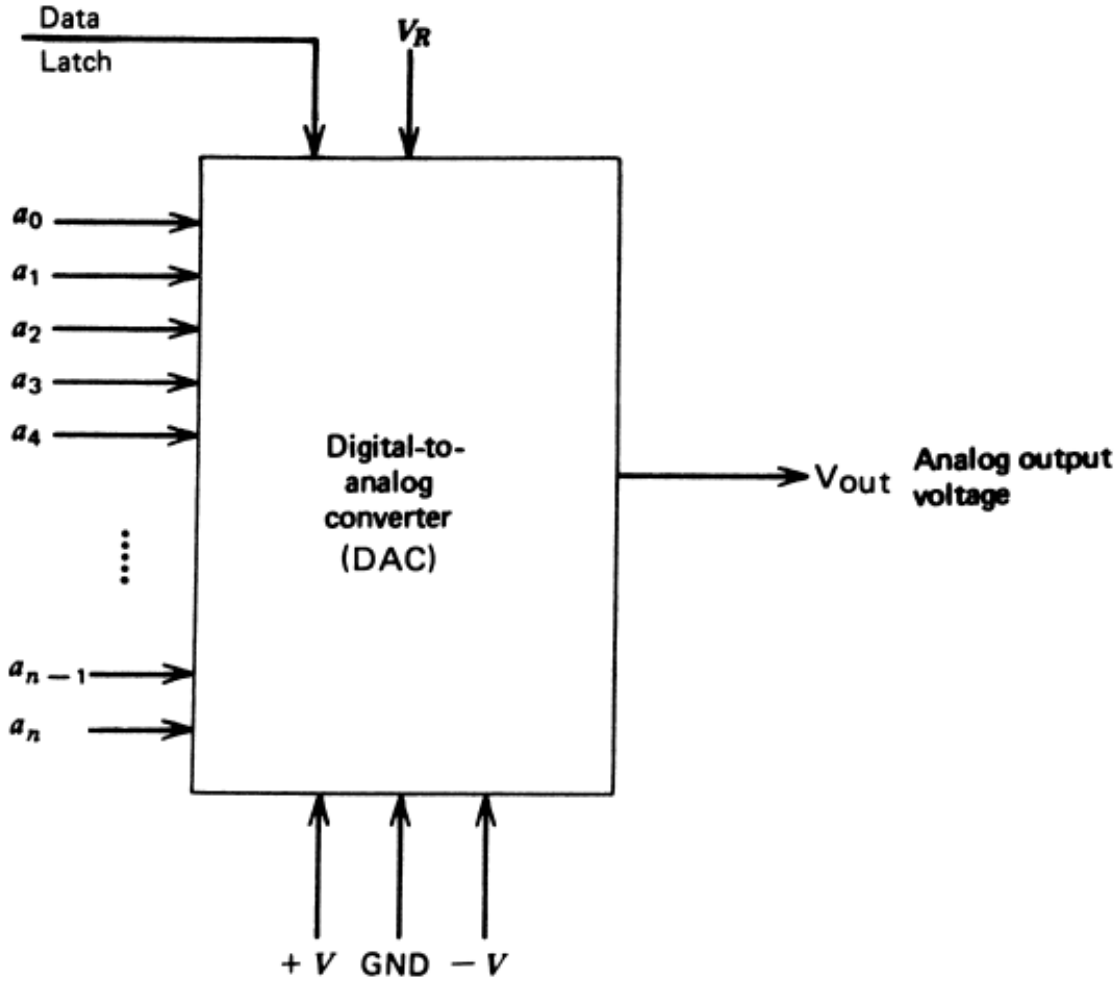
$$(R/R_f)\,(5\ \text{V}) = 150\ \text{mV}$$
$$(R/R_f) = 0.03$$

Let:

$$R_f = 100\ \text{k}\Omega, \text{ then } R = 3\ \text{k}\Omega.$$

Digital-to-Analog Converters (DACs)

- A DAC accepts digital information and transforms it into an analog voltage.
- The digital information is in the form of a binary number with some fixed number of digits.



A unipolar DAC

- A unipolar DAC converts a digital word into an analog voltage by scaling the analog output to be zero when all bits are zero and some maximum value when all bits are one.

$$V_{out} = V_R[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}]$$

where V_{out} = analog voltage output
V_R = reference voltage
$b_1 b_2 \ldots b_n$ = n-bit binary word
N = base 10 whole-number equivalent of DAC input

$$V_{out} = \frac{N}{2^n} V_R$$

- The minimum output is 0 volt
- The maximum output depends on the V_R and n.
- The conversion resolution is the change in analog output for a 1-bit change in binary word

$$\Delta V_{out} = V_R 2^{-n}$$

A unipolar DAC

EXAMPLE 9 What is the output voltage of a 10-bit DAC with a 10.0-V reference if the input is **(a)** 0010110101_2 = 0B5H, **(b)** 20FH? What input is needed to get a 6.5-V output?

Solution

Let's use Equation (5) for part **(a)** and Equation (6) for part **(b)**. Thus, for the 0B5H input, we have

$$V_{out} = 10.0[2^{-3} + 2^{-5} + 2^{-6} + 2^{-8} + 2^{-10}]$$
$$V_{out} = 10.0[0.1767578]$$
$$V_{out} = 1.767578 \text{ V}$$

For **(b)**, we have $20FH = 527_{10}$ and $2^{10} = 1024$, so

$$V_{out} = (527/1024)10.0$$
$$V_{out} = (0.514648)10.0$$
$$V_{out} = 5.14648 \text{ V}$$

We can use Equation (6) to determine the input needed to get a 6.5-V output by solving for N,

$$N = 2^n(V_{out}/V_R)$$
$$N = 1024(6.5/10)$$
$$N = 665.6$$

The fact that there is a fractional remainder tells us that we cannot get exactly 6.5 V from the converter. The best we can do is get an output for $N = 665 = 299\,\text{H}$ or $666 = 29\,\text{AH}$. The outputs for these two inputs are 6.494 V and 6.504 V, respectively. The only way to get exactly 6.5 V of output would be to change the value of the reference slightly.

A Bipolar DAC

- Some DACs are designed to output a voltage that ranges from plus to minus some maximum when the input binary ranges over the counting states.
- A simple offset-binary is frequently used.

$$V_{out} = \frac{N}{2^n} V_R - \frac{1}{2} V_R$$

$$V_{out}(\max) = \frac{(2^n - 1)}{2^n} V_R - \frac{1}{2} V_R = \frac{1}{2} V_R - \frac{V_R}{2^n}$$

$$V_{out}(\min) = -V_R/2$$

Bipolar DAC

EXAMPLE 10 A bipolar DAC has 10 bits and a reference of 5 V. What outputs will result from inputs of 04FH and 2A4H? What digital input gives a zero output voltage?

Solution

The inputs of 04FH and 2A4H can easily be converted to base 10 numbers 79_{10} and 676_{10}. Then, from Equation (7), we find

$$V_{out} = \frac{79}{1024}(5) - \frac{(5)}{2} = -2.1142578 \text{ V}$$

$$V_{out} = \frac{676}{1024}(5) - \frac{(5)}{2} = 0.80078 \text{ V}$$

The zero occurs when Equation (7) equals zero. Solving for N gives

$$0 = \frac{N}{1024}(5) - \frac{(5)}{2}$$

or $N = 512_{10} = 200\,\text{H} = \mathbf{1000000000_2}$.

EXAMPLE 11 Determine how many bits a D/A converter must have to provide output increments of 0.04 V or less. The reference is 10 V.

$$\Delta V_{OUT} = \frac{V_R}{2^n} = 0.04 \Rightarrow 2^n = \frac{10}{0.04} = 250$$

$$n \log 2 = \log 250 \Rightarrow n = 7.96$$

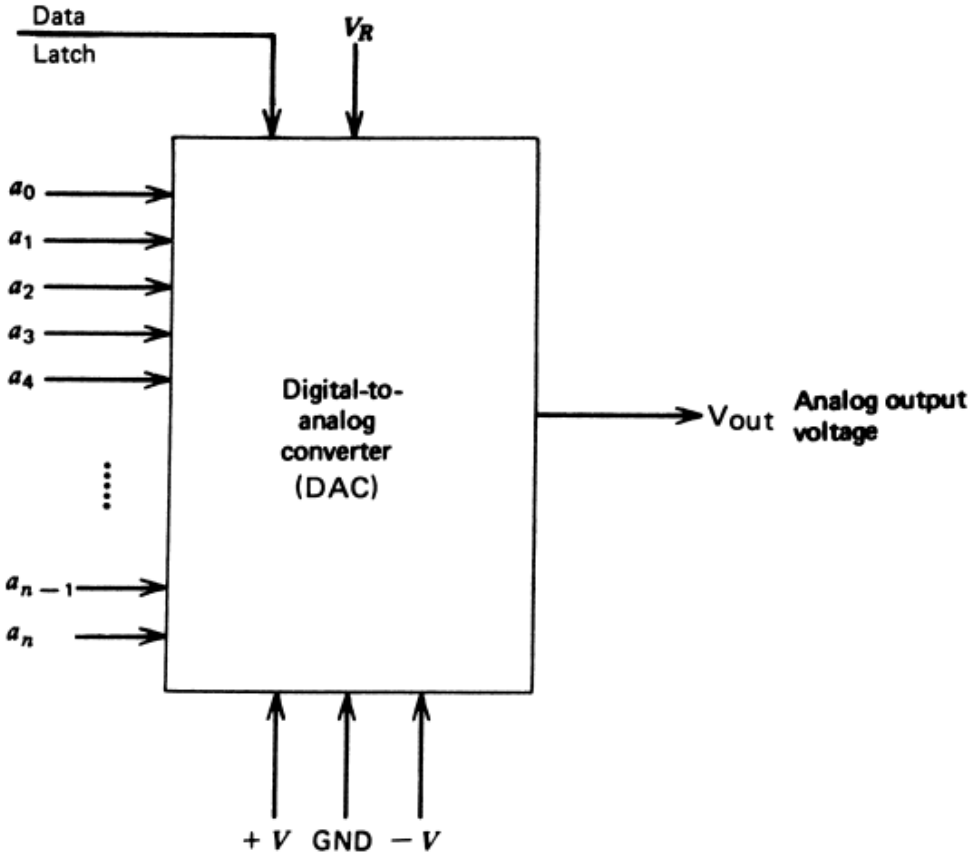
Take $n = 8$ bits

because $n = 8$ give $\Delta V = 0.039$ → best resolution

but $n = 7$ give $\Delta V = 0.07$ (X)

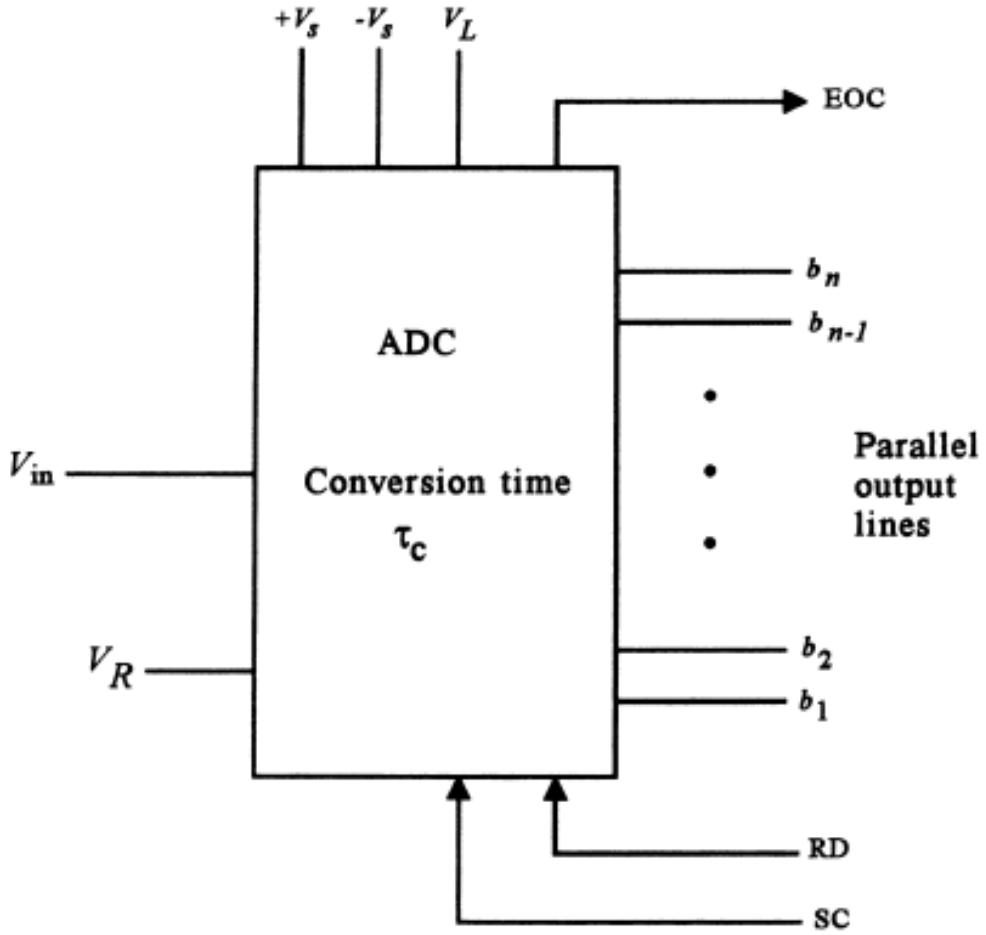
DAC Characteristics

- Digital Input (usually TTL logic levels)
- Power Supply (single - Bipolar)
- Ref. Voltage (internal –external)
- Output (unipolar – Bipolar)
- Data latch Microprocessor compatible
- Conversion time very small (typically msec.)



Analog-to-Digital Converters (ADCs)

- Although there are sensors that provide a direct digital signal output and more are being develop, most still convert the measured variable into an analoged, electrical signal.
- With the growing use of digital logic and computers in process control, it is necessary to employ an ADC to provide a digitally encoded signal for the computer.



A unipolar ADC

- The ADC will find a fractional binary number that gives the closest approximation to the fraction formed by the input voltage and reference.

$$b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n} \leq \frac{V_{\text{in}}}{V_R}$$

- The only way the left side can change is if the input fraction changes by only 2^{-n} and nothing in between.
- Therefore, there is an inherent uncertainty in the input voltage

$$\Delta V = V_R 2^{-n}$$

- The fractional binary number can be expressed as

$$N = \text{INT}\left(\frac{V_{\text{in}}}{V_R} 2^n\right)$$

A unipolar ADC

EXAMPLE 13 Temperature is measured by a sensor with an output of 0.02 V/°C. Determine the required ADC reference and word size to measure 0° to 100°C with 0.1°C resolution.

Solution

At the maximum temperature of 100°C, the voltage output is

$$(0.02\ \text{V/°C})\,(100\text{°C}) = 2\ \text{V}$$

so a 2-V reference is used.

A change of 0.1°C results in a voltage change of

$$(0.1\text{°C})\,(0.02\ \text{V/°C}) = 2\ \text{mV}$$

so we need a word size where

$$0.002\ \text{V} = (2)\,(2^{-y})$$

$$y = 9.996 \approx 10$$

A unipolar ADC

EXAMPLE 15 The input to a 10-bit ADC with a 2.500-V reference is 1.45 V. What is the hex output? Suppose the output was found to be 1B4H. What is the voltage input?

Solution

We will use Equation (11) to find the solution to these questions. For the first part, we can form the expression

$$N = \text{INT}((1.45/2.5)2^{10})$$
$$N = \text{INT}(593.92)$$
$$N = 593$$
$$N = 251\,\text{H}$$

So the output of the ADC is 251H for a 1.45-V input. To get the voltage input for a 1B4H-output, we solve Equation (11) for the voltage:

$$V_{\text{in}} = \frac{N}{2^n} V_R$$

A conversion yields $1B4H = 436_{10}$.

$$V_{\text{in}} = (436/1024)2.50$$
$$V_{\text{in}} = 1.06445\ \text{V}$$

However, it is important to realize that any voltage from this to $1.06445 + 2.5/1024 = 1.06689$ will give the same output, 1B4H. So the correct answer to the question is that the input voltage lies in the range 1.06445 to 1.06689 V.

Bipolar ADC

- A bipolar ADC is one that accepts bipolar input voltage for conversion
- The most common bipolar ADCs provide an output called offset binary.

$$N = \text{INT}\left[\left(\frac{V_{\text{in}}}{V_R} + \frac{1}{2}\right)2^n\right]$$

$$V_{\text{in}} = -V_R/2 \longrightarrow N = 0$$

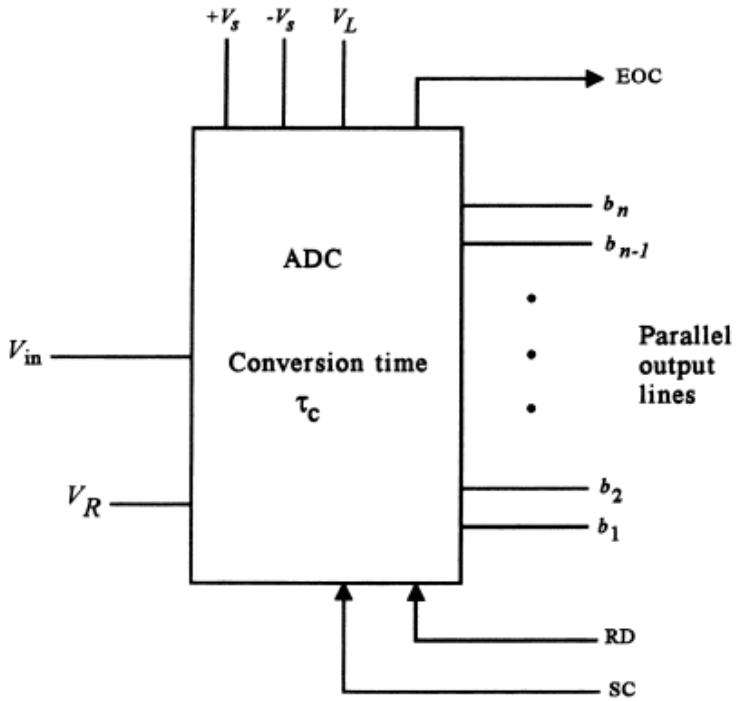
$$V_{\text{in}} = 0 \longrightarrow N = 10000000_2$$

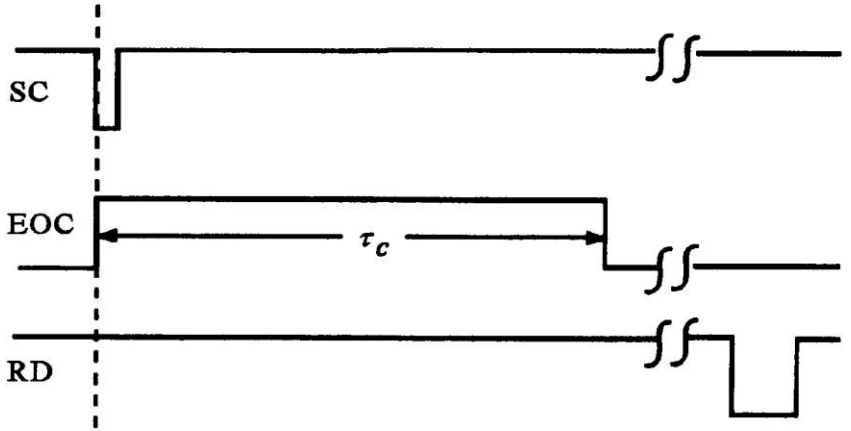
$$V_{\text{in}} = \frac{1}{2}V_R - \frac{V_R}{2^n} \longrightarrow N = 11111111_2$$

Check Ex.16

ADC Characteristics

- Input must be stable during conversion.
- Power supplies
- Reference voltage (stable well regulated internal/external).
- Control lines (SC- EOC- RD)
  - SC (Start-convert): this is a digital input to the ADC that starts the converter on the process of finding the correct digital outputs for the given analog voltage input.
  - EOC (End-of-convert): When the conversion is complete, the line will go low. This is a digital output from the ADC to receiving equipment.
  - RD (Read): The receiving equipment must take the RD line low to enable the tri-states and place the data on the output lines.
- Conversion time: The ADC must sequence through a process to find the appropriate digital output, and this process takes time.





Conversion Time Consequences

- The finite conversion time of the ADC has serious consequences on the rate of change of signals presented for conversion.
- An ADC performs the conversion process by referring back to the input signal while the conversion is taking place. Obviously, if the input is changing while this process is taking place, errors will occur.
- There is a solution, however. What is needed is simply that the signal not changing during the conversion process.
- Therefore, the answer is to hold the value constant during that process. This is accomplished with a sample-and-hold (S/H) circuit.

$$\frac{dV_{\text{in}}}{dt} \leq \frac{\Delta V}{\tau_c} = \frac{V_R}{2^n \tau_c}$$

$$V_{\text{in}} = V_0 \sin(\omega t)$$

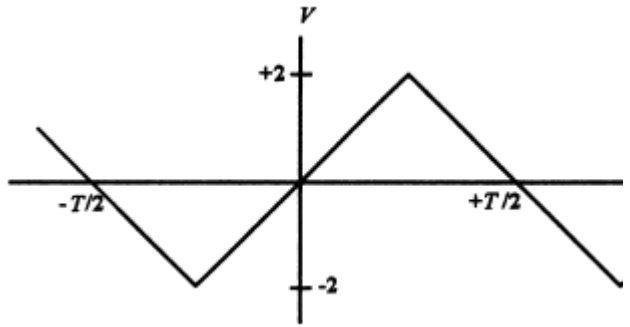
$$\omega V_0 \cos(\omega t) \leq \frac{V_R}{2^n \tau_c}$$

$$\omega \leq \frac{V_R}{2^n \tau_c V_0}$$

$$f \leq \frac{V_R}{2^{n+1} \pi \tau_c V_0}$$

Conversion Time Consequences

EXAMPLE 20 An 8-bit, bipolar ADC with a 5-V reference will be used to take samples of a triangular wave as shown in Figure 19. What is the maximum frequency of the wave if the ADC conversion time is 12 μs?



Solution

The solution is found from the condition expressed by Equation (18). From Figure 19 it is clear that the derivative of the input signal is simply the slope of the triangular wave,

$$\frac{dV_{\text{in}}}{dt} = \frac{2}{T/4} = \frac{8}{T} = 8f$$

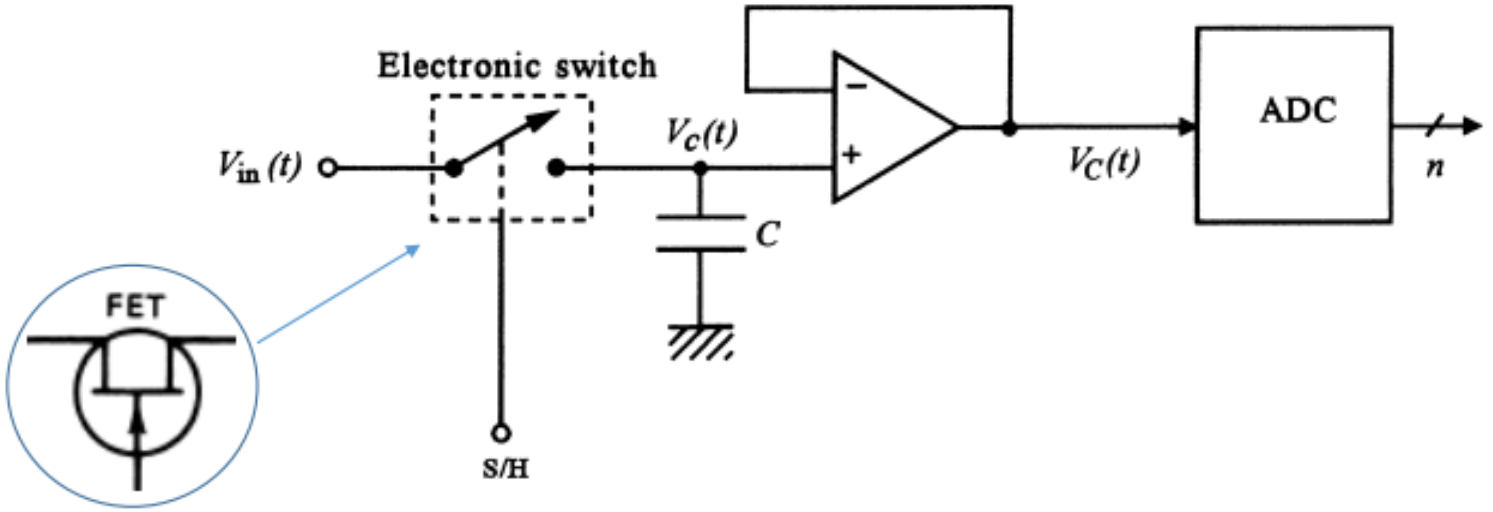
where T is the period and f is the frequency. Then, from Equation (18),

$$8f \leq \frac{5}{2^8(12 \times 10^{-6})} = 1627.6 \text{ Hz}$$

or $f \leq 203.5$ Hz.

Sample-and-Hold

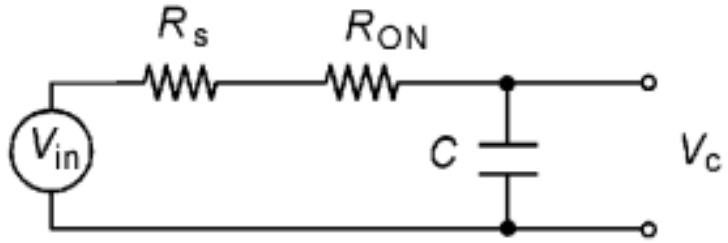
- When SC is low S/H electronic switch is opened → the capacitor holds the charge.
- When EOC is low S/H electronic switch is closed → the capacitor charges
- The voltage follower (very high input impedance)



Practical Sample-and-Hold

- When S/H electronic switch is closed (Sampling)
  - Low-pass limitation:

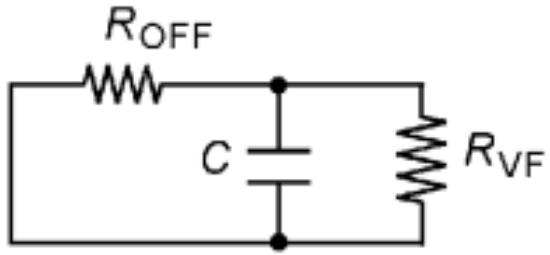
$$f_c = \frac{1}{2\pi(R_s + R_{ON})C}$$



a) Sampling

  - Most commercial S/H circuits reduce this limitation by using a voltage follower before the switch, since it has very low output resistance.
- When S/H electronic switch is opened (Holding)

$$\tau_D = \frac{R_{OFF}R_{VF}}{R_{OFF} + R_{VF}}C \qquad \frac{V_C}{\tau_D} \le \frac{V_R}{2^n\tau_c} \qquad \tau_D \ge 2^n\tau_c\frac{V_C}{V_R}$$



b) Holding

Practical Sample-and-Hold

EXAMPLE 21 A S/H will be used with a 12-bit, unipolar ADC with a 30-μs conversion time. The S/H switch ON resistance is 10 Ω, and its OFF resistance is 10 MΩ. The voltage follower input resistance is also 10 MΩ, while the signal source output resistance is 50 Ω.

a. What value of capacitor should be used?

b. Determine the sampling cutoff frequency.

Solution

a. Equation (24), under the worst-case condition that $V_C = V_R$ will determine the minimum droop time, $\tau_D \geq 2^{12}(30 \times 10^{-6}) = 0.12288$ s. Now Equation (22) will allow determination of C,

$$\frac{(10^7)(10^7)}{(10^7 + 10^7)} C \geq 0.12288$$

which gives $C \geq 0.025\ \mu$F.

b. From this result and Equation (22), the critical frequency during sampling is found to be

$$f_c = \frac{1}{(2\pi)(50 + 10)(0.025 \times 10^{-6})} = 108 \text{ kHz}$$

Sampling Frequency

- **Acquisition time t_{acq}** It is the time required for the S/H to reacquire the signal when changing from hold to sample mode. (OFF→ ON)
- **Aperture time t_{ap}** It is the time between when a command to hold is given and the actual signal level is held. (ON→ OFF)
- Then minimum time between samples is

$$T = \tau_c + \tau_{\text{acq}} + \tau_{\text{ap}}$$

or max. throughput frequency

$$f_{\max} = 1/T.$$

Check Ex.22

Try this problem:

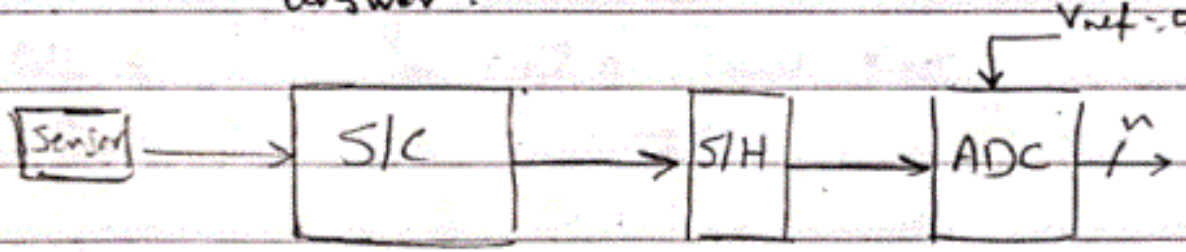
Mid term 2013:-

- Felix has become the first skydiver to go faster than the speed of sound reaching a max velocity of (1342 km/h). in jumping out of balloon (39 km) above earth, also smashed the record for the highest ever free fall
- As an electronic engineer, you are asked to design an altitude (height) measurement system for this mission. The require resolution is (10 m) and the altitude sensor used has a T.f (0.1 mV/m) from the block diagram of the suggested system shown, find:-

(a) Design a suitable S/C Ot

(b) what is the min. number of bits (n) of ADC?

(c) τ_c = 10 msec, are you need S/H Ot or not? prove your answer.



END OF LECTURE

BEST WISHES